VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES

9. A printed wiring board comprising a dielectric substrate, at least one filled plated through hole having an outside diameter, formed by the steps of:

(a) depositing a seed layer on a planar surface of said dielectric substrate and on a surface defined by a hole through said dielectric substrate;

(b) depositing electrically conductive plating having a thickness on said planar surface of said dielectric substrate and on said surface defined by said hole to form a subcomposite;

(c) filling said hole with a filler composition;

(d) etching said subcomposite to partially remove said electrically conductive layer and thereby reducing the electrically conductive plating thickness to a minimum thickness of about 0.2 mil.;

(e) removing residual amounts of said filler composition on said subcomposite; and

(f) etching said subcomposite to completely remove said electrically conductive plating; and

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circuitry on said dielectric substrate connecting to said plated through hole, said circuitry having circuit lines having a line width approximately equal to or less than the diameter of said filled plated through hole, wherein the circuitry is formed by the steps of:

(g) depositing a seed activator on the surface of said subcomposite including said filler composition;

(h) covering said subcomposite with a photoresist and exposing and developing said photoresist to reveal selected areas of said subcomposite including the filler composition; and

(i) additively plating electrical circuitry on said selected areas of said subcomposite including circuitry on said filler composition electrically connected to the electrically conductive plating on the surface defined by the hole.

10. A printed wiring board comprising a dielectric substrate, at least one filled plated through hole, formed by the steps of:

(a) depositing a seed layer on a planar surface of said dielectric substrate and on a surface defined by a hole through said dielectric substrate;

(b) depositing electrically conductive plating on said planar surface of said dielectric substrate and on said surface defined by said hole to form a subcomposite;

(c) filling said hole with a filler composition;

(d) etching said subcomposite to partially remove said electrically conductive layer;

(e) removing residual amounts of said filler composition on said subcomposite; and

(f) etching said subcomposite to completely remove said electrically conductive plating; and

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circuitry on said dielectric substrate connecting to said plated through hole, said circuitry having circuit lines, the circuit lines having an aspect ratio greater than about 0.5, wherein the circuitry is formed by the steps of:

(g) depositing a seed activator on the surface of said subcomposite including said filler composition;

(h) covering said subcomposite with a photoresist and exposing and developing said photoresist to reveal selected areas of said subcomposite including the filler composition; and

(i) additively plating electrical circuitry on said selected areas of said subcomposite including circuitry on said filler composition electrically connected to the electrically conductive plating on the surface defined by the hole.

11. A printed wiring board comprising a dielectric substrate, at least one filled plated through hole, and circuitry on said dielectric substrate connecting to said plated through hole, said circuitry having an aspect ratio greater than about 1.

12. The invention as defined in claim 9 wherein said circuitry includes a pad on each of said filled plated through holes, wherein each pad diameter is about equal the filled plated through hole diameter.

13. The invention as defined in claim 10 wherein said circuitry includes a pad on each of said filled plated through holes.

14. The invention as defined in claim 11 wherein said circuitry includes a pad on each of said filled plated through holes.

15. The invention as defined in claim 9 further characterized by a layer of dielectric material disposed on said dielectric substrate and overlying said circuitry on said dielectric substrate, said layer of dielectric material having at least one via formed therein.

16. The invention as defined in claim 10 further characterized by a layer of dielectric material disposed on said dielectric substrate and overlying said circuitry on said dielectric substrate, said layer of dielectric material having at least one via formed therein.

17. The invention as defined in claim 11 further characterized by a layer of dielectric material disposed on said dielectric substrate and overlying said circuitry on said dielectric substrate, said layer of dielectric material having at least one via formed therein.

18. The invention as defined in claim 15 further characterized by circuitry disposed on a top surface of said layer of dielectric material.

19. The invention as defined in claim 16 further characterized by circuitry disposed on a top surface of said layer of dielectric material.

20. The invention as defined in claim 17 further characterized by circuitry disposed on a top surface of said layer of dielectric material.

21. (New) The invention as defined in claim 11, wherein the filled plated through hole is formed by the steps of:

(a) depositing a seed layer on a planar surface of said dielectric substrate and on a surface defined by a hole through said dielectric substrate;

(b) depositing electrically conductive plating on said planar surface of said dielectric substrate and on said surface defined by said hole to form a subcomposite;

(c) filling said hole with a filler composition;

(d) etching said subcomposite to partially remove said electrically conductive layer;

(e) removing residual amounts of said filler composition on said subcomposite; and

(f) etching said subcomposite to completely remove said electrically conductive plating; and

wherein the circuitry is formed by the steps of:

(g) depositing a seed activator on the surface of said subcomposite including said filler composition;

(h) covering said subcomposite with a photoresist and exposing and developing said photoresist to reveal selected areas of said subcomposite including the filler composition; and

(i) additively plating electrical circuitry on said selected areas of said subcomposite including circuitry on said filler composition electrically connected to the electrically conductive plating on the surface defined by the hole.